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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,300	07/25/2003	Jeong Ho Park	OF03P107/US	1904

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,300	PARK, JEONG HO	
	Examiner	Art Unit	
	Lex Malsawma	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 9 and 20 are objected to because of the following informalities:

At claim 9, line 3, the examiner suggests deleting "a" before "nitride layers".

Claim 20 is a duplicate of claim 16.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 7, 11-16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woerlee et al. (6,406,963 B2; hereinafter, "**Woerlee**") in view of **Wu** (5,856,226).

Regarding claims 1 and 11:

Woerlee discloses a method of forming short-channel transistors, the method comprising the steps of:

forming a first oxide layer 7 and a sacrificial layer ***8 (consisting essentially of polysilicon, Col. 5, lines 37-38)*** one after another on a semiconductor substrate 1 and etching the sacrificial layer, thus forming a residual sacrificial layer pattern 10 (Fig. 1 and Col. 5, lines 31-35);

conducting an ion implantation using the residual sacrificial layer pattern 10 as a mask, thus forming an LDD ion-implant layer 11 in the semiconductor substrate (Fig. 1 and Col. 5, lines 54-55);

forming first spacers 13 on both side walls of the sacrificial layer pattern 10 (Fig. 2);

conducting an ion implantation using the residual sacrificial layer pattern 10 and the first spacers as a mask, thus forming a source/drain ion-implant layer 14/15 under the LDD ion-implant layer 11 (Figs. 1-2);

forming a nitride layer 17 and a second oxide layer 18 one after another on the whole surface of the former resultant object (NOTE: annealing must be performed after ion-implant layers 14/15 are formed in order to activate the dopants, therefore, this limitation is not considered to carry patentable weight);

conducting ***a*** CMP process to the extent that an upper surface of the residual sacrificial layer pattern 10 is exposed (Fig. 4 and Col. 6, lines 26-32), and removing the residual sacrificial layer pattern 10 through etching (Fig. 6 and Col. 6, lines 34-52);

conducting an ion implantation 22 on the substrate ***through the first oxide layer 7 (Col. 7, lines 37-41)***, thus forming a punch-stop ion implant layer 20 (Fig. 6);

etching the first oxide layer 7 under the portion where the residual sacrificial layer pattern 10 is removed, and forming a gate insulating layer 24 (Figs. 6-7; Col. 6, lines 42-43; and Col. 7, lines 25-26); and

forming a gate 21 where the residual sacrificial layer pattern is removed (Fig. 11 and Col. 8, lines 34-35).

Woerlee **lacks** forming second spacers on side walls of a portion where the residual sacrificial layer pattern is removed; conducting the punch-stop ion implantation between the second spacers; ***and forming the gate on the second spacers***. Wu **teaches** a method for forming ultra-short channel transistors, wherein the method allows the formation of a gate width narrower than lithographic limitations (Col. 5, lines 55-62). Wu disclose the method comprises forming spacers 20 within a recess portion having an oxide 12 formed therein (Fig. 3); conducting an ion implantation between the spacers 20 ***and the oxide 12*** to form a punch-stop ion implant layer 24 (Fig. 3 and Col. 5, lines 63-65); etching the oxide 12 and forming a gate insulation layer 28 (Figs. 4-5 and Col. 6, lines 6-16); and forming a gate 30 ***on the second spacers*** (Fig. 6). Wu discloses (in col. 1, lines 15-60) background information explaining why ultra-short channel transistors are an important aspect of high-speed ULSI circuits. Accordingly, it would have been obvious to one of ordinary skill in the art to modify Woerlee by incorporating spacers and punch-stop implantation, as taught by Wu, because such a modification would provide an ultra-short channel transistor ***with a gate width narrower than a width achievable by a lithographic process***.

Regarding claims 2-4, 7, 12 and 13:

Woerlee discloses ***the residual sacrificial layer pattern 8 is removed by wet etching (Col. 6, lines 44-48) where*** the first oxide layer 7 is used as an etch stop layer when etching the sacrificial layer to form the residual sacrificial layer pattern 10 (see Fig. 1); the gate insulation layer 24 (Fig. 7) and the gate 21 (Fig. 11) are formed after the source/drain regions 14/15 are previously formed (Fig. 2); the sacrificial layer is formed of polysilicon 8 (Fig. 1); and using the

first oxide layer as buffer layer when ion implanting the LDD 11 and the source/drain 14/15 (Figs. 1-2).

Regarding claim 5:

Woerlee (in view of Wu) discloses the claimed invention except for the second oxide being multi-layered. However, applicant has not disclosed that a multi-layered oxide is for any particular purpose or solves any stated problem (note specification, page 6, lines 12-15), and it appears that the invention would perform equally well with a "single" oxide layer (as disclosed by Woerlee). In other words, if so desired, one could modify Woerlee by replacing the second oxide layer with multi-layers of oxides, oxides-and-nitrides, oxide-nitride-oxides, etc., however, no significant improvement in the manufacturing process (or device performance) would be apparent, but rather, it would seem that processing time would be needlessly increased; therefore, this claim is held obvious over the cited references, especially since one of ordinary skill in the art could obviously choose to incorporate numerous "time consuming" process steps that serve no particular purpose (if so desired).

Regarding claims 14-16 and 20:

These claims are similar to claims 1 and 4 with the only significant being that, in claim 14, a limitation exists for etching the exposed first oxide layer, and forming a gate insulating layer. Woerlee, modified as taught by Wu, discloses etching the exposed first oxide layer and forming a gate insulating layer, then forming a gate on the gate insulating layer and the second spacers. Note that Wu discloses (in Figs. 3-6) etching an exposed first oxide layer 12 (Figs. 3-4); forming a gate insulation layer 28 (Fig. 5); and forming a gate 30 (Fig. 6) on the gate insulation

layer and the spacers 20. Therefore, these claims are held obvious over the cited references with reasoning similar to those state above in reference to claims 1 and 4.

Regarding claim 19:

Woerlee discloses (in Figs.10-11 and Col. 8, lines 10-11) the gate forming step comprises depositing a polysilicon layer 30 on a whole surface of a structure following the gate insulation layer forming step, and planarizing the polysilicon layer to form the gate. Wu discloses a similar process form forming a gate (note Figs. 4-6 and Col. 6, lines 34-48). Therefore, this claim is rendered obvious by the cited references.

4. Claims 6, 8-10, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Woerlee** (in view of **Wu**) as applied to claims 1 and 14 above, and further in view of Yu et al. (6,180,468 B1; hereinafter, "**Yu**").

Regarding claim 6:

Woerlee (in view of Wu) discloses all limitations in these claims (see above, in section "5", *Regarding claim 1*) ***except for the punch-stop ion implant layer being adapted as a threshold-voltage adjustment ion implant layer and the first and second spacers each consisting essentially of a nitride layer***. Yu **teaches** a method that provides an ultra-low thermal budget process for channel implant (note Col. 2, lines 17-31), ***wherein the process steps are very similar to that disclosed by Woerlee (in view of Wu). More specifically, Yu discloses*** the method comprising the steps of: removing a residual sacrificial layer pattern 24 (Figs. 2-3); forming second spacers 32/34 where the residual pattern 24 is removed (Fig. 4); and conducting an ion implantation adapted as a threshold-voltage adjustment ion-implant layer (Figs. 4-5). Yu

discloses the criticality of reducing process thermal budget (note Col. 1, line 48 to Col. 2, line 14); ***and since Yu's process is very similar to that disclosed by Woerlee (in view of Wu)***, it would have been obvious to one of ordinary skill in the art to modify Woerlee (in view of Wu) by ***adapting the punch-stop ion implant layer as a threshold-voltage adjustment ion implant layer (as taught by Yu)*** because the modification would allow a significant reduction in process thermal budget and allow the acquisition of a sharp transition in the doping profile within the channel region (note Yu, paragraph bridging Cols. 1-2).

Regarding claims 8-10:

Yu discloses first spacers 26/28 and second spacers 32/34 being formed of nitride layers (Fig. 4 and Col. 3, lines 15-16 and 34-39). Therefore, these claims are held obvious over the cited references.

Regarding claims 17 and 18:

Woerlee (in view of Wu) discloses the method of claim 14 but **lacks** the first spacers consisting of nitride and the second spacers also consisting of nitride. Although Woerlee (modified as taught by Wu) specifically discloses first spacers 13 formed of oxide (Woerlee, Col. 5, lines 64-67) and second spacers 20 formed of nitride (Wu, Col. 5, lines 51-53), Yu **teaches** that both first 26/28 and second 32/34 spacers (Fig. 4), utilized in a manufacturing process very similar to that disclosed by Woerlee (in view of Wu), can consist essentially of nitride. In other words, oxides and nitrides are very well known materials utilized for spacers, and at least Yu teaches/shows that nitride can be readily incorporated for both first and second spacers within a process very similar to that disclosed by Woerlee (in view of Wu); accordingly, it would have been obvious to one of ordinary skill in the art to modify Woerlee (in view of Wu) by utilizing

nitride (instead of oxide) for the first spacers 13 in combination with the second nitride spacers 20 because Yu shows that utilizing nitride for both first and second spacers would provide a "double" spacer structure that functions in a manner essentially the same as the "double" spacer structure utilized by Woerlee (in view of Wu); furthermore, since oxides and nitrides are well known suitable materials for spacers, modifying Woerlee (in view of Wu) by using nitride instead of oxide for the first spacers is considered to an obvious matter of selecting a known material on the basis of its suitability—Note that it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Remarks

Applicant's remarks/arguments have been carefully reviewed and considered, but they are not persuasive for the following reasons. Applicant asserts there is no reason, suggestion, or motivation found in Woerlee and/or Wu to combine these references. It seems that Applicant has ignored the reasoning provided by in the prior Office Action for combining the references, and instead of addressing the reasoning previously provided (and currently repeated), Applicant seems to search for reasons why one of ordinary skill in the art would not be motivated to combine the references. As stated above, in reference to claims 1 and 11, a reason and motivation clearly exist for combining the references because Woerlee modified as taught by Wu would clearly provide an ultra-short channel transistor with a gate width narrower than a width achievable by a lithographic process. Furthermore, Woerlee already provides LDD and source/drain implant layers such that no significant changes would have to made to Woerlee's

process flow when Wu's teaching is incorporated into Woerlee. In other words, Wu's process steps for forming an ultra-short channel (and gate) can be easily and readily incorporated into Woerlee because the "second" spacers 20 taught by Wu would be formed just before Woerlee's step of forming the punch-stop layer 20, and the subsequent steps taught by Wu (shown in Figs. 4-6) will readily follow without disrupting (or adversely affecting) the remaining process steps within Woerlee's method. When Woerlee is modified as taught by Wu, the punch-stop implant layer will occupy a smaller area within the channel region because the punch-stop implant layer will be self-aligned with the second spacers 20 (note Wu, Fig. 3); therefore, Applicant's assertion, *"there may also be reasons understood by those of ordinary skill in the art not to form a punch stop implant layer through spacers in a substrate that already has LDD and source/drain implant layers therein"*, is supposition not supported by the facts, especially because the smaller area occupied by the punch-stop implant layer (acquired by Woerlee in view of Wu) would surely provide more room/area for the atoms in the punch-stopping implant layer to diffuse, or migrate, during any subsequent, extensive annealing, i.e., if Woerlee (alone) successfully forms a punch-stopping implant layer in a substrate that already has LDD and source/drain implant layers, then the smaller-area-occupying punch-stop layer, acquired when Woerlee is modified as taught by Wu, would surely not be affected by the issues raised by the Applicant because there will be even more room/area available for the atoms to diffuse, or migrate, in comparison to the room/area available in the process disclosed by Woerlee (alone). (note the issues raised by Applicant's remarks in the two paragraphs bridging pages 12-13).

Applicant's remarks/arguments in reference to the prior combination of Woerlee and Yu are moot in view of the new grounds of rejections introduced for at least claims 6, 8 and 9, where the new grounds of rejections were necessitated by Applicant's amendment.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

March 11, 2005

OLIK CHAUDHURI
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